REMARKS

Claims 4-6, 8-16 and 18-20 were pending in the Application. Applicants reinstate originally filed claims 1-3, 7 and 17 as added claims 21-25, respectively. Therefore, claims 4-6, 8-16 and 18-25 are pending in the Application.

As discussed in the previous response (April 30, 2007), Applicants cancelled claims 1-3, 7 and 17 in order to expedite the issuance of claims 4-6, 8-16 and 18-20 which were indicated as allowable. However, the Examiner has now rejected claims 4-6, 8-16 and 18-20 in the present Office Action. Applicants will address herein the rejections of the claims that were presented in the prior Office Action (4/2/2007) and in the present Office Action (6/19/2007).

Applicants thank the Examiner for discussing the Office Actions with Applicants' Attorney, Bobby Voigt, on August 21, 2007.

I. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH:

The Examiner has rejected claims 24 and 25[1] under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. Office Action (4/2/2007), page 2. In particular, the Examiner asserts that a multiplexor is the essential element that has been omitted. *Id.* Applicants respectfully traverse the assertion that claims 24 and 25 are incomplete for omitting essential elements.

Applicants respectfully assert that claims 24 and 25 purposely recite a limitation directed to not having a multiplexer coupled between the bit line and the latch. The muliplexor recited in claims 24 and 25 is not an essential element as there is not a muliplexor coupled between the bit line and the latch. Applicants respectfully assert that claims 24 and 25 do not omit matter disclosed to be essential to the invention as described in the Specification. Accordingly, claims 24 and 25 are allowable under 35 U.S.C. §112, second paragraph.

Furthermore, a rejection for omitting essential elements is not appropriate under 35 U.S.C. §112, second paragraph. M.P.E.P. §2172.01. Instead, such a

[1] Claims 24 and 25 correspond to originally filed claims 7 and 17, respectively.

rejection is appropriate under 35 U.S.C. §112, first paragraph. M.P.E.P. §2172.01. Accordingly, claims 24-25 are allowable under 35 U.S.C. §112, second paragraph.

II. REJECTIONS UNDER 35 U.S.C. §102(e):

The Examiner has rejected claims 1-3 and 7[2] under 35 U.S.C. §102(e) as being anticipated by Amatangelo et al. (U.S. Patent Application Publication No. 2003/0009318) (hereinafter "Amatangelo"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicants respectfully assert that Amatangelo does not disclose "a latch coupled to the bit line" as recited in claim 21. The Examiner cites "bit" in Figure 12 of Amantangelo as disclosing the claimed bit line. Office Action (4/2/2007), page 3. The Examiner further cites element 1302 in Figure 13 of Amantangelo as disclosing the claimed latch. *Id.* Applicants respectfully traverse the assertion that Amantangelo discloses the above-cited claim limitation.

Amantangelo instead discloses that Figure 13 shows details of one of the read multiplexers 1104. [0047]. Amantangelo further discloses that the multiplexer circuitry includes a precharge and latch 1310 for cluster output node 1111 and a precharge and latch 1302 for cluster output node 1112. [0047]. Hence, Amantangelo discloses a read multiplexer 1104 that includes a precharge and latch 1302 for cluster output node 1112.

As illustrated in Figures 11 and 12 of Amantangelo, read multiplexer 1104 is not coupled to the bit line indicated as "bit" (Examiner asserts that the bit line indicated as "bit" corresponds to the claimed bit line). Thus, Amantangelo does not disclose all of the limitations of claim 21, and thus Amantangelo does not anticipate claim 21. M.P.E.P. §2131.

[2] Originally filed claims 1-3 and 7 corresponds to claims 21-24, respectively.

Applicants further assert that Amatangelo does not disclose "an inverter coupled between an output of the latch and the bit line" as recited in claim 21. The Examiner had previously cited element 1302 in Figure 13 of Amatangelo as disclosing the claimed latch. Office Action (4/2/2007), page 3. Further, the Examiner had previously cited "bit" in Figure 12 of Amantangelo as disclosing the claimed bit line. *Id.* The Examiner further cites element 1306 in Figure 13 of Amatangelo as disclosing the claimed inverter. Office Action (4/2/2007), page 3. Additionally, the Examiner cites paragraph [0048] of Amantangelo as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

Amatangelo instead discloses that the two in precharge and latch circuits 1301 and 1302 are identical and include a precharge P-type transistor P1303, pull-up and pull-down transistors P1304 and N1305, respectively, and a feedback inverter 1306. [0047]. Hence, Amatangelo discloses that feedback inverter 1306 is within precharge and latch circuit 1302, which the Examiner had previously identified as disclosing the claimed latch.

The Examiner is in essence citing the same element in Amatangelo as disclosing both the claimed latch and the claimed inverter. This is improper and makes no sense. How can the same element be an inverter coupled between an output of itself (latch) and the bit line? The Examiner must cite to different elements in Amatangelo as disclosing these two separate elements (inverter and latch). Thus, Amantangelo does not disclose all of the limitations of claim 21, and thus Amantangelo does not anticipate claim 21. M.P.E.P. §2131.

Further, there is no depiction in Figure 13 or description of Figure 13 that discloses that inverter 1306 is coupled between an output of precharge and latch circuit 1302 (Examiner asserts that precharge and latch circuit 1302 discloses the claimed latch) and the bit line indicated as "bit" (Examiner asserts that the bit line indicated as "bit" corresponds to the claimed bit line). Thus, Amantangelo does not disclose all of the limitations of claim 21, and thus Amantangelo does not anticipate claim 21. M.P.E.P. §2131.

Claims 22-24 each recite combinations of features of independent claim 21, and thus claims 22-24 are not anticipated by Amantangelo for at least the above-stated reasons that claim 21 is not anticipated by Amantangelo.

Claims 22-24 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Amantangelo.

For example, Amantangelo does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 23. The Examiner cites element 1117 in Figure 13 of Amantangelo as disclosing the above-cited claim limitation. Office Action (4/2/2007), page 3. Applicants respectfully traverse.

Amantangelo instead discloses that element 1117 corresponds to the mux output for multiplexer 1104. [0046]. Thus, Amantangelo does not disclose that the output of the precharge and latch circuit 1302 (Examiner asserts that precharge and latch circuit 1302 discloses the claimed latch) is an output of the register file. Thus, Amantangelo does not disclose all of the limitations of claim 23, and thus Amantangelo does not anticipate claim 23. M.P.E.P. §2131.

Applicants further assert that Amantangelo does not disclose "wherein a multiplexor is not coupled between the bit line and the latch" as recited in claim 24. The Examiner cites to multiplexer 1104 of Amantangelo as disclosing the above-cited claim limitation. Office Action (4/2/2007), page 3. Applicants respectfully traverse.

The above-cited claim limitation recites a multiplexer not coupled between the bit line and the latch. Hence, the citing to a multiplexer of Amantangelo does not disclose the above-cited claim limitation. Thus, Amantangelo does not disclose all of the limitations of claim 24, and thus Amantangelo does not anticipate claim 24. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Amantangelo, and thus claims 21-24 are not anticipated by Amantangelo. M.P.E.P. §2131.

III. REJECTIONS UNDER 35 U.S.C. §102(b):

The Examiner has rejected claims 4 and 11-13[3] under 35 U.S.C. §102(b) as being anticipated by Ho (U.S. Patent No. 5,629,901). Further, the Examiner has rejected claims 4-6[4] under 35 U.S.C. §102(b) as being anticipated by Chung et al. (U.S. Patent No. 5,590,087) (hereinafter "Chung"). Additionally, the Examiner has rejected claims 4-6 and 8-20[5] under 35 U.S.C. §102(b) as being anticipated by Raje (U.S. Patent No. 6,105,123). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

A. Claims 4, 11-13 and 21-23 are not anticipated by Ho.

Applicants respectfully assert that Ho does not disclose "a plurality of register file cells coupled to a bit line" as recited in claim 11 and similarly in claim 21. The Examiner cites elements 24 and BL in Figure 4 as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 2. Applicants respectfully traverse.

Ho instead discloses that Figure 4 is a schematic diagram of the write portion for the multi-write port register cell according to the present invention. Column 1, lines 63-65; Column 3, lines 13-14. Figure 4 does not depict a plurality of register cells. Thus, Ho does not disclose all of the limitations of claims 11 and 21, and thus Ho does not anticipate claims 11 and 21. M.P.E.P. §2131.

Applicants further assert that if the Examiner is asserting that element 24 corresponds to a register cell, Applicants respectfully traverse. Ho discloses that each of the write port WLs 1 through w (associated with each entry) are connected to corresponding ones of the sources of the FETs 24_1 to 24_n, and the drains of the FETs are connected in common to the input of the latch formed by cross-coupled inventers

[3] Applicants will also address the limitations of claims 21-23.
[4] Applicants will also address the limitations of claims 21-23.
[5] Applicants will also address the limitations of claims 21-23.

21 and 22. Column 2, lines 58-62. The Examiner must provide a basis in fact and/or technical reasoning to support the assertion that FETs 24 of Ho correspond to register file cells. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that FETs 24 of Ho correspond to register file cells, and that it would be so recognized by persons of ordinary skill. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided any such objective evidence, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 11 and 21. M.P.E.P. §2131.

Further, Applicants are confused over the citing of element BL in Figure 4 in connection with the rejection of the above-cited claim limitation. Applicants agree that it corresponds to a bit line; however, claims 11 and 21 recite a plurality of register file cells coupled to a bit line. Figure 4 depicts the write portion of a single register cell. Applicants request clarification of the rejection pursuant to 37 C.F.R. §1.104(c)(2).

Applicants further assert that Ho does not disclose "a latch coupled to the bit line" as recited in claim 11 and similarly in claim 21. The Examiner cites elements 21, 22 in Figure 4 of Ho as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 2. Applicants respectfully traverse the assertion that Ho discloses the above-cited claim limitation.

Ho discloses that cross-coupled inverters 21 and 22, form a latch. Column 2, lines 44-45. However, Figure 2 does not show that the latch formed by cross-coupled inverters 21 and 22 is coupled to a bit line which is coupled to a plurality of register file cells. Thus, Ho does not disclose all of the limitations of claims 11 and 21, and thus Ho does not anticipate claims 11 and 21. M.P.E.P. §2131.

Applicants further assert that Ho does not disclose "a transmission gate circuit coupled between an output of the latch and the bit line" as recited in claim 11. The Examiner cites element 31 in Figure 4 of Ho as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse.

Ho instead discloses that a new FET, 31, has been added to the cell that now functions as the singular Write-Enable gate for the cell. Column 3, lines 16-18.

There is no language in Ho that discloses that FET 31 corresponds to a transmission gate circuit. Neither is there any language in Ho that discloses that FET 31 corresponds to a transmission gate circuit coupled between an output of a latch and a bit line. Instead, Ho discloses that FET 31 is coupled to the input of the latch formed by cross-coupled inverters 21 and 22 as illustrated in Figure 4. Thus, Ho does not disclose all of the limitations of claim 11, and thus Ho does not anticipate claim 11. M.P.E.P. §2131.

Applicants further assert that Ho does not disclose "an inverter coupled between an output of the latch and the bit line" as recited in claim 21. The Examiner cites elements 44 and "LCB" in Figure 5 as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 2. Applicants respectfully traverse.

Ho instead discloses that element 44 corresponds to a tri-state buffer 44 which receives as its input the system clock signal. Column 3, lines 42-44.

As illustrated in Figure 5, tri-state buffer 44 is not coupled between an output of the latch (Examiner had asserted that elements 21 and 22 of Ho formed the claimed latch) and the bit line coupled to a plurality of register file cells. Further, tri-state buffer 44 is not coupled to the bit line designated as "BL" which the Examiner had previously cited as allegedly disclosing the claimed bit line. Additionally, the Examiner now appears to be citing to a different element ("LCB") as disclosing the claimed bit line. Applicants request clarification pursuant to 37 C.F.R. §1.104(c)(2). Thus, Ho does not disclose all of the limitations of claim 21, and thus Ho does not anticipate claim 21. M.P.E.P. §2131.

Claims 4 and 22-23 each recite combinations of features of independent claim 21, and thus claims 4 and 22-23 are not anticipated by Ho for at least the above-stated reasons that claim 21 is not anticipated by Ho.

Further, claims 12 and 13 each recite combinations of features of independent claim 11, and thus claims 12 and 13 are not anticipated by Ho for at least the above-stated reasons that claim 11 is not anticipated by Ho.

Claims 4, 12-13 and 22-23 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Ho.

For example, Ho does not disclose "wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter" as recited in claim 4.

Applicants further assert that Ho does not disclose "an inverter coupled between the bit line and an input of the latch" as recited in claim 12. The Examiner cites Figures 8 and 10 of Ho as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse.

There is no depiction in Figures 8 and 10 that discloses an inverter coupled between the bit line and an input of the latch. Thus, Ho does not disclose all of the limitations of claim 12, and thus Ho does not anticipate claim 12. M.P.E.P. §2131.

Applicants further assert that Ho does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 13. The Examiner cites Figure 10 of Ho as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse.

There is no depiction in Figure 10 that discloses that the output of the latch is an output of the register file. Thus, Ho does not disclose all of the limitations of claim 13, and thus Ho does not anticipate claim 13. M.P.E.P. §2131.

Applicants further assert that Ho does not disclose "another inverter coupled between the bit line and an input of the latch" as recited in claim 22. Applicants further assert that Ho does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 23.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Ho, and thus claims 4, 11-13 and 21-23 are not anticipated by Ho. M.P.E.P. §2131.

B. Claims 4-6 and 21-23 are not anticipated by Chung.

Applicants respectfully assert that Chung does not disclose "a latch coupled to the bit line" as recited in claim 21. The Examiner cites elements 2E, 520 and 521 of Chung as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse the assertion that Chung discloses the above-cited claim limitation.

Applicants have performed a search for the elements 2E, 520 and 521 in Chung and were unable to locate them. Applicants respectfully request clarification pursuant to 37 C.F.R. §1.104(c)(2). Further, there is no depiction in Figure 1 of a latch coupled to a bit line coupled to a plurality of register file cells. Thus, Chung does not disclose all of the limitations of claim 21, and thus Chung does not anticipate claim 21. M.P.E.P. §2131.

Applicants further assert that Chung does not disclose "an inverter coupled between an output of the latch and the bit line" as recited in claim 21. The Examiner cites element 106 and column 2, lines 60-65 of Chung as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse.

Applicants have performed a search for the element 106 in Chung and was unable to locate it. Applicants respectfully request clarification pursuant to 37 C.F.R. §1.104(c)(2).

Further, Chung instead discloses that the stability of memory cells are at risk during read operations because bit lines could potentially overwrite a stored bit in the memory cell during read operations if both read bit line levels are not high enough prior to access. Column 2, lines 59-63. Chung further discloses that when the memory design is used for the multi-ported register file, cell stability is of particular concern because the pull down to pass gate size ratio will be different depending on how many ports are accessed at the same time. Column 2, lines 63-67.

There is no language in the cited passage that discloses an inverter coupled between an output of the latch and the bit line. Thus, Chung does not disclose all of

the limitations of claim 21, and thus Chung does not anticipate claim 21. M.P.E.P. §2131.

Claims 4-6 and 22-23 each recite combinations of features of independent claim 21, and thus claims 4 and 22-23 are not anticipated by Chung for at least the above-stated reasons that claim 21 is not anticipated by Chung.

Claims 4-6 and 22-23 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Chung.

For example, Chung does not disclose "wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter" as recited in claim 4. The Examiner cites column 3, lines 14-20 of Chung as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse.

Chung instead discloses that one known solution to the cell stability problem has been used with a multi-ported register file having 17 ports to ensure sufficient bit line precharge levels. Column 3, lines 14-16. Chung further discloses that this solution has the disadvantages of requiring additional precharge pulse generation circuitry which will generate a lot of noise that further complicates the cell stability problem. Column 3, lines 16-19.

There is no language in the cited passage that discloses an inverter that is a tri-state inverter receiving a hold select signal to control operation of the inverter. Thus, Chung does not disclose all of the limitations of claim 4, and thus Chung does not anticipate claim 4. M.P.E.P. §2131.

Applicants further assert that Chung does not disclose "wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch" as recited in claim 5. The Examiner cites elements 3, 40, 44 and 46 of Chung as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse.

Chung instead discloses that each write port 24 includes a pass gate 44 which is activated by a write word line (WWL) to supply a bit on a write bit line (WBL) to

the internal node A for storage in the memory cell 10. Column 5, lines 61-63. Chung additionally discloses that the read ports 26 include pass gates 46 which are activated by the read word lines (RWL). Column 5, line 66 – column 6, line 1.

There is no language in the description of elements 44 and 46 of Chung that discloses an output of the inverter is coupled to the bit line and where an input of the inverter is coupled to the output of the latch. Thus, Chung does not disclose all of the limitations of claim 5, and thus Chung does not anticipate claim 5. M.P.E.P. §2131.

Further, Applicants could not locate elements 3 and 40 of Chung. Applicants respectfully request clarification pursuant to 37 C.F.R. §1.104(c)(2).

Applicants further assert that Chung does not disclose "wherein data is read out of the register array to be input into the latch" as recited in claim 6. The Examiner cites element 523 of Chung as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 3. Applicants respectfully traverse.

Applicants have performed a search for element 523 in Chung and was unable to locate it. Applicants respectfully request clarification pursuant to 37 C.F.R. §1.104(c)(2). Further, there is no depiction in Figure 1 that discloses data that is read out of the register array to be input into the latch. Thus, Chung does not disclose all of the limitations of claim 6, and thus Chung does not anticipate claim 6. M.P.E.P. §2131.

Applicants further assert that Chung does not disclose "another inverter coupled between the bit line and an input of the latch" as recited in claim 22. Applicants further assert that Chung does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 23.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Chung, and thus claims 4-6 and 21-23 are not anticipated by Chung. M.P.E.P. §2131.

C. Claims 4-6, 8-20 and 21-23 are not anticipated by Raje.

Applicants respectfully assert that Raje does not disclose "an inverter coupled between an output of the latch and the bit line" as recited in claim 21. The Examiner

cites Figure 2 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 4. Applicants respectfully traverse.

There is no description of Figure 2 that discusses an inverter coupled between an output of the latch and the bit line. Thus, Raje does not disclose all of the limitations of claim 21, and thus Raje does not anticipate claim 21. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "a latch with its input coupled to the global bit line" as recited in claim 8 and similarly in claim 18. The Examiner cites element 104 of Figure 5 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 5. Applicants respectfully traverse.

Raje instead discloses that in register file 100, pipestage register 104 and tristate driver 106 are interposed sense amp 54 and the GLOBAL BIT LINE. Column 5, lines 30-32. Hence, Raje discloses that element 104 corresponds to a pipestage register.

There is no language in the description of element 104 of Raje that discloses that pipeline register 104 corresponds to a latch. Neither is there any language in Raje that discloses that pipeline register 104 has its input coupled to a global bit line. Thus, Raje does not disclose all of the limitations of claims 8 and 18, and thus Raje does not anticipate claims 8 and 18. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "a third tri-state inverter coupled between an output of the latch and the global bit line, the third tri-state inverter controlled by a hold signal" as recited in claim 8. The Examiner cites elements 64 and 92 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 5. Applicants respectfully traverse.

Raje instead discloses that element 64 corresponds to a sense amplifier as illustrated in Figures 4 and 5. Column 2, lines 46-46. Sense amplifier 64 does not correspond to a tri-state inverter. Further, the Examiner had previously cited element 92 (enable logic) of Raje as disclosing the first and second local select signal. Office Action (6/19/2007), pages 4-5. Applicants respectfully request clarification as to how element 92 also discloses the claimed hold signal, which is another element, pursuant

to 37 C.F.R. §1.104(c)(2). Further, there is no indication in Figures 4-5 of Raje of sense amplifier 64 being controlled by a hold signal. Further, there is no indication in Figures 4-5 of Raje of sense amplifier 64 being controlled by enable logic 92 of Raje. Thus, Raje does not disclose all of the limitations of claim 8, and thus Raje does not anticipate claim 8. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "a transmission gate circuit coupled between an output of the latch and the bit line" as recited in claim 11. The Examiner cites element "Z" in Figure 2 of Raje as disclosing the claimed latch; element "BITLINE" in Figure 2 of Raje as disclosing the claimed bit line and elements "CLK, transistors, inverter" in Figure 2 of Raje as disclosing the claimed transmission gate circuit. Office Action (6/19/2007), page 5. Applicants respectfully traverse the assertion that Raje discloses the above-cited claim limitation.

There is no depiction in Figure 2 or description of Figure 2 that discloses that the "CLK, transistors, inverter" pointed out by the Examiner corresponds to a transmission gate circuit. Neither is there any depiction in Figure 2 or description of Figure 2 that discloses that the "CLK, transistors, inverter" pointed out by the Examiner corresponds to a transmission gate circuit coupled between an output of latch and the bit line. Thus, Raje does not disclose all of the limitations of claim 11, and thus Raje does not anticipate claim 11. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "a first transmission gate coupled between the first local bit line and the global bit line, the first transmission gate controlled by a first local select signal; a second transmission gate coupled between the second local bit line and the global bit line, the second transmission gate controlled by a second local select signal; a third transmission gate coupled between an output of the latch and the global bit line, the third transmission gate controlled by a hold signal" as recited in claim 18. The Examiner has not specifically addressed these limitations. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d

1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed these limitations, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 18. M.P.E.P. §2131.

Claims 4-6 and 22-23 each recite combinations of features of independent claim 21, and thus claims 4-6 and 22-23 are not anticipated by Raje for at least the above-stated reasons that claim 21 is not anticipated by Raje.

Further, claims 9-10 each recite combinations of features of independent claim 8, and thus claims 9-10 are not anticipated by Raje for at least the above-stated reasons that claim 8 is not anticipated by Raje.

Additionally, claims 12-17 each recite combinations of features of independent claim 11, and thus claims 12-17 are not anticipated by Raje for at least the above-stated reasons that claim 11 is not anticipated by Raje.

Further, claims 19-20 each recite combinations of features of independent claim 18, and thus claims 19-20 are not anticipated by Raje for at least the above-stated reasons that claim 18 is not anticipated by Raje.

Claims 4-6, 9-10, 12-17, 19-20 and 22-23 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Raje.

For example, Raje does not disclose "wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter" as recited in claim 4. The Examiner cites elements 92 and 106 in Figure 5 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 4. Applicants respectfully traverse.

There is no depiction in Figure 5 that tri-state driver 106 is coupled between an output of the latch and the bit line. Claim 4 depends from claim 21, and the "inverter" referred to in claim 4 refers to the inverter coupled between the output of the latch and the bit line, as required by claim 21. Thus, Raje does not disclose all of the limitations of claim 4, and thus Raje does not anticipate claim 4. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch" as recited in claim 5. The Examiner cites to Figure 2 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 4. Applicants respectfully traverse.

There is no depiction in Figure 2 of Raje that discloses an output of an inverter coupled to the bit line coupled to a plurality of register file cells. Neither is there any depiction in Figure 2 of Raje that discloses an input of the inverter coupled to the output of the latch. Thus, Raje does not disclose all of the limitations of claim 5, and thus Raje does not anticipate claim 5. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein data is read out of the register array to be input into the latch" as recited in claim 6. The Examiner cites to Figure 2 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 4. Applicants respectfully traverse.

There is no depiction in Figure 2 of Raje that discloses that data is read out of the register array to be input into the latch. Thus, Raje does not disclose all of the limitations of claim 6, and thus Raje does not anticipate claim 6. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "an inverter coupled between the global bit line and the input of the latch" as recited in claim 9. The Examiner cites Figure 1 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 5. Applicants respectfully traverse.

There is no depiction in Figure 1 of Raje that discloses an inverter coupled between a global bit line and an input of a latch. Thus, Raje does not disclose all of the limitations of claim 9, and thus Raje does not anticipate claim 9. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein when the third tri-state inverter is activated, the first and second local select signals are deactivated" as recited in claim 10. The Examiner has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently

describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 10. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 13. The Examiner previously cited to element "Z" in Figure 2 of Raje as disclosing the claimed latch. Office Action (6/19/2007), page 5. The Examiner further cites Figure 5 of Raje as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

There is no depiction in Figure 5 or description of Figure 5 that discloses an output of a latch being an output of the register file. Neither is there any depiction in Figure 5 or description of Figure 5 that discloses that the output of element "Z" in Figure 2 is an output of the register file. Thus, Raje does not disclose all of the limitations of claim 13, and thus Raje does not anticipate claim 13. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein the transmission gate circuit receives a hold select signal" as recited in claim 14. The Examiner had previously cited to the "CLK, inverter, transistors" in Figure 2 of Raje as disclosing the claimed transmission gate circuit. Office Action (6/19/2007), page 5. The Examiner further cites element 92 of Figure 5 as disclosing the above-cited claim limitation. *Id.* Applicants respectfully traverse.

There is no depiction in Figure 5 or description of Figure 5 that discloses a transmission gate circuit receiving a hold select signal. Neither is there any depiction in Figure 5 or description of Figure 5 that discloses that the "CLK, inverter, transistors" in Figure 2 (Examiner asserts that such elements discloses the claimed transmission gate circuit) receives a hold select signal. Thus, Raje does not disclose all of the limitations of claim 14, and thus Raje does not anticipate claim 14. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is coupled to the output of the latch" as recited in claim 15.

The Examiner cites Figure 2 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 5.

There is no depiction in Figure 2 or description of Figure 2 that discloses an output of a transmission gate circuit that is coupled to the bit line. Neither is there any depiction in Figure 2 or description of Figure 2 that discloses that an input of a transmission gate circuit is coupled to an output of a latch. Thus, Raje does not disclose all of the limitations of claim 15, and thus Raje does not anticipate claim 15. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein data is read out of the register array to be input into the latch" as recited in claim 16. The Examiner cites Figure 2 of Raje as disclosing the above-cited claim limitation. Office Action (6/19/2007), page 5.

There is no depiction in Figure 2 or description of Figure 2 that discloses that data is read out of the register array to be input into a latch. Thus, Raje does not disclose all of the limitations of claim 16, and thus Raje does not anticipate claim 16. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "an inverter coupled between the global bit line and the input of the latch" as recited in claim 19. The Examiner has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 19. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "wherein when the third transmission gate is activated, the first and second local select signals are deactivated" as recited in claim 20. The Examiner has not specifically addressed this limitation. The Examiner is reminded that in order to establish a *prima facie* case of anticipation, the Examiner must provide a single prior art reference that expressly or inherently

describes each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Since the Examiner has not addressed this limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 19. M.P.E.P. §2131.

Applicants further assert that Raje does not disclose "another inverter coupled between the bit line and an input of the latch" as recited in claim 22. Applicants further assert that Raje does not disclose "wherein the output of the latch is an output of the register file" as recited in claim 23.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Raje, and thus claims 4-6, 8-20 and 21-23 are not anticipated by Raje. M.P.E.P. §2131.

IV. CONCLUSION:

As a result of the foregoing, it is asserted by Applicants that claims 4-6, 8-16 and 18-25 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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